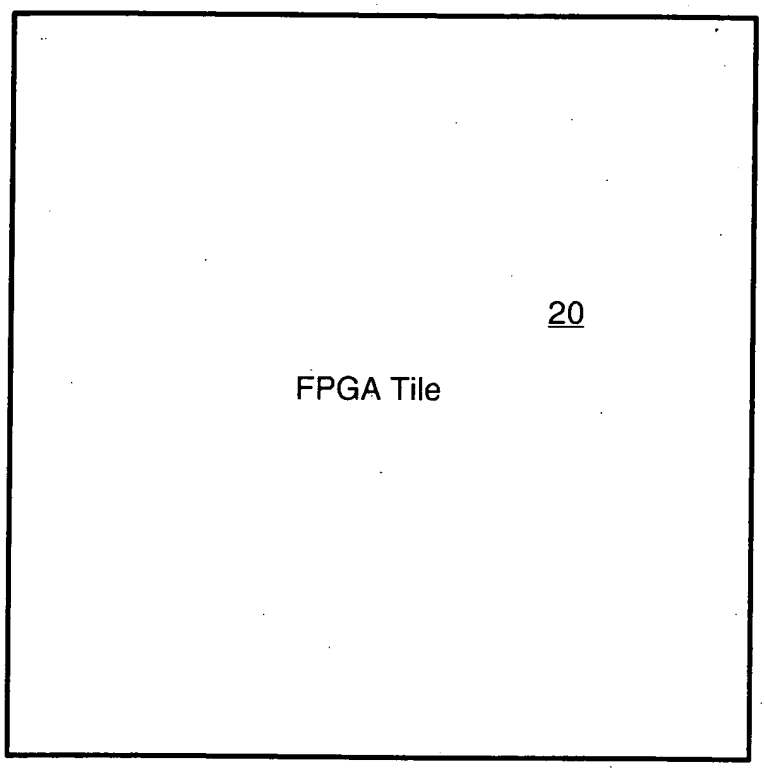

FIG. 1

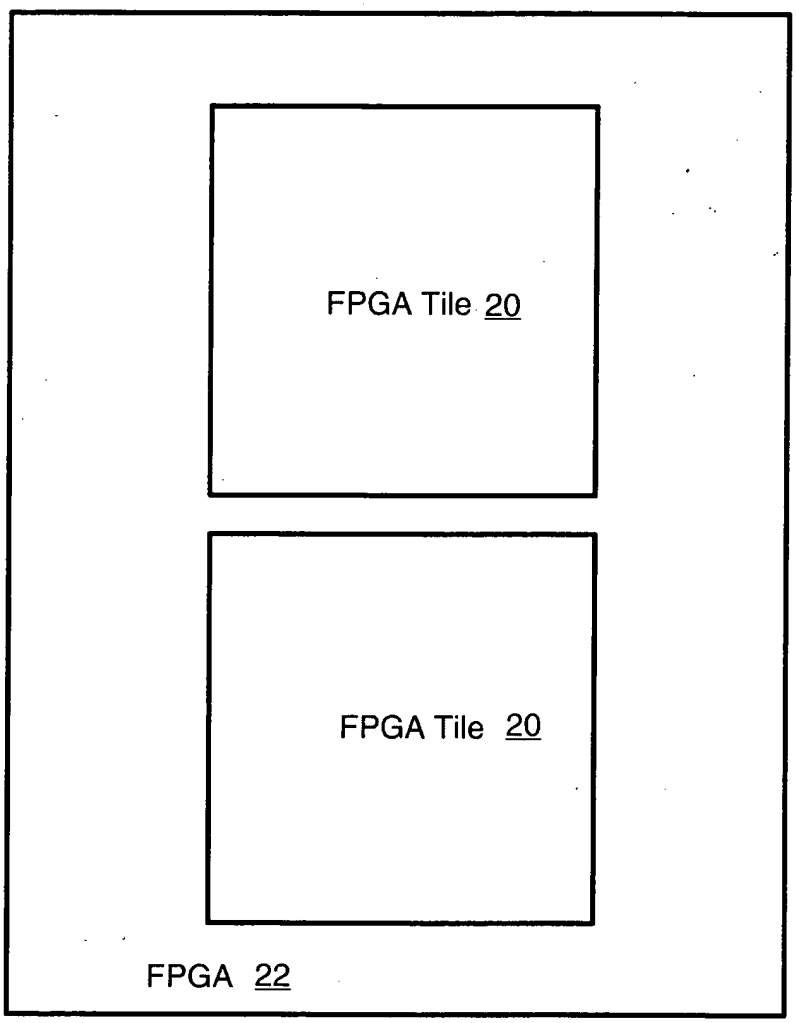

FIG. 2

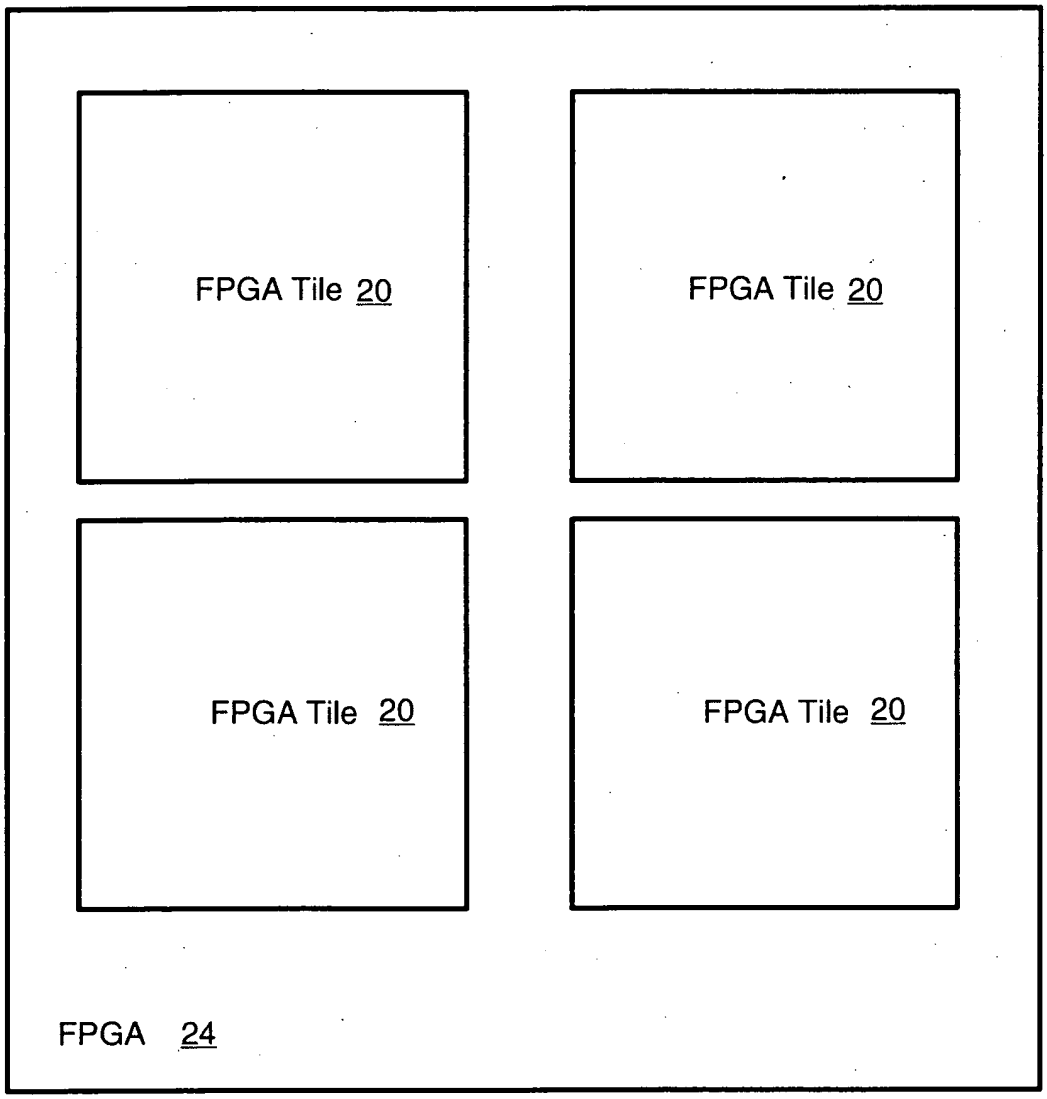

FIG. 3A

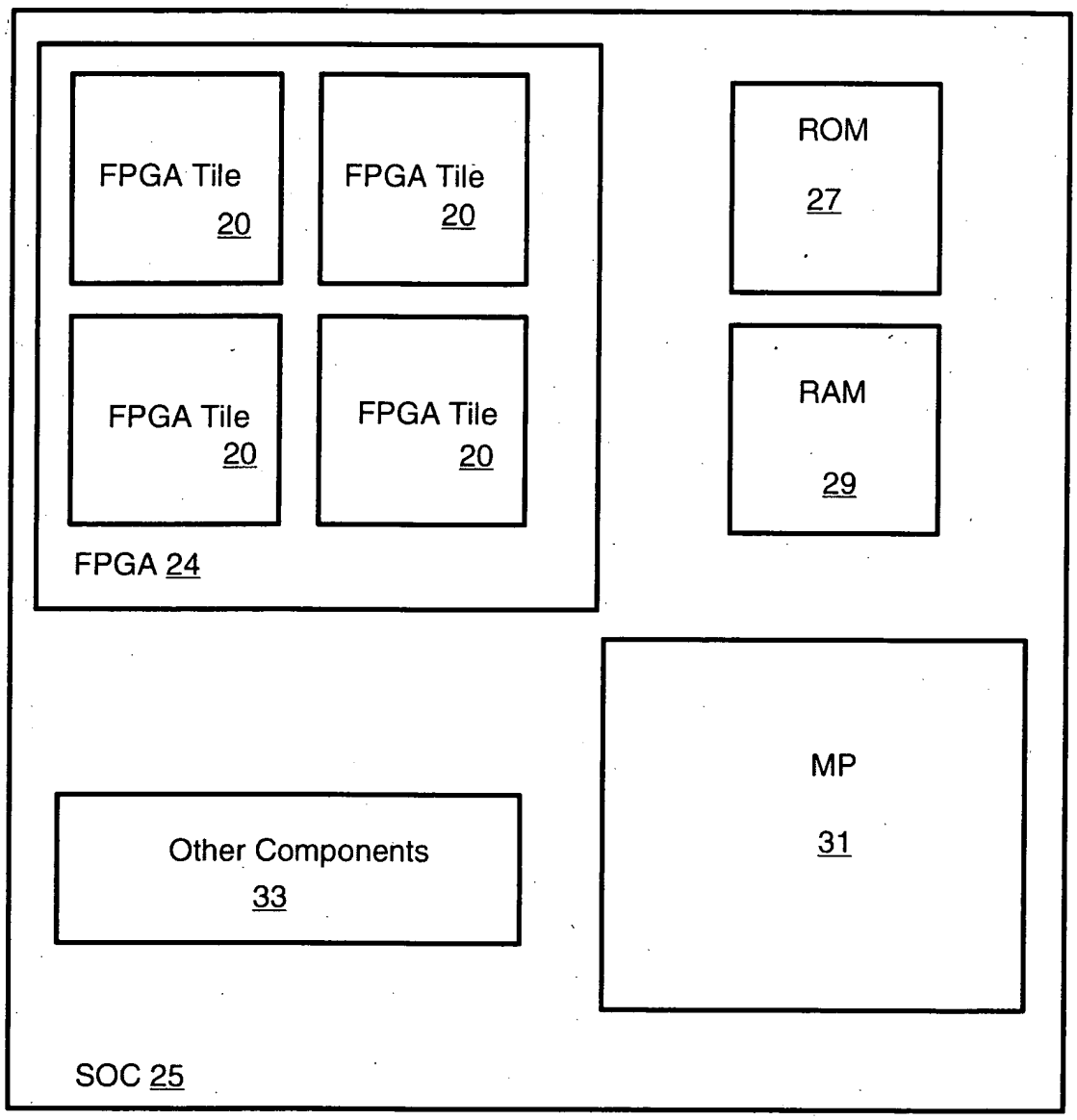
FPGA Tile
20
FPGA Tile
20
FPGA Tile
20
FPGA Tile
20
FPGA 24
ROM
27
RAM
29
MP
31
Other Components
33
SOC 25

FIG. 3B

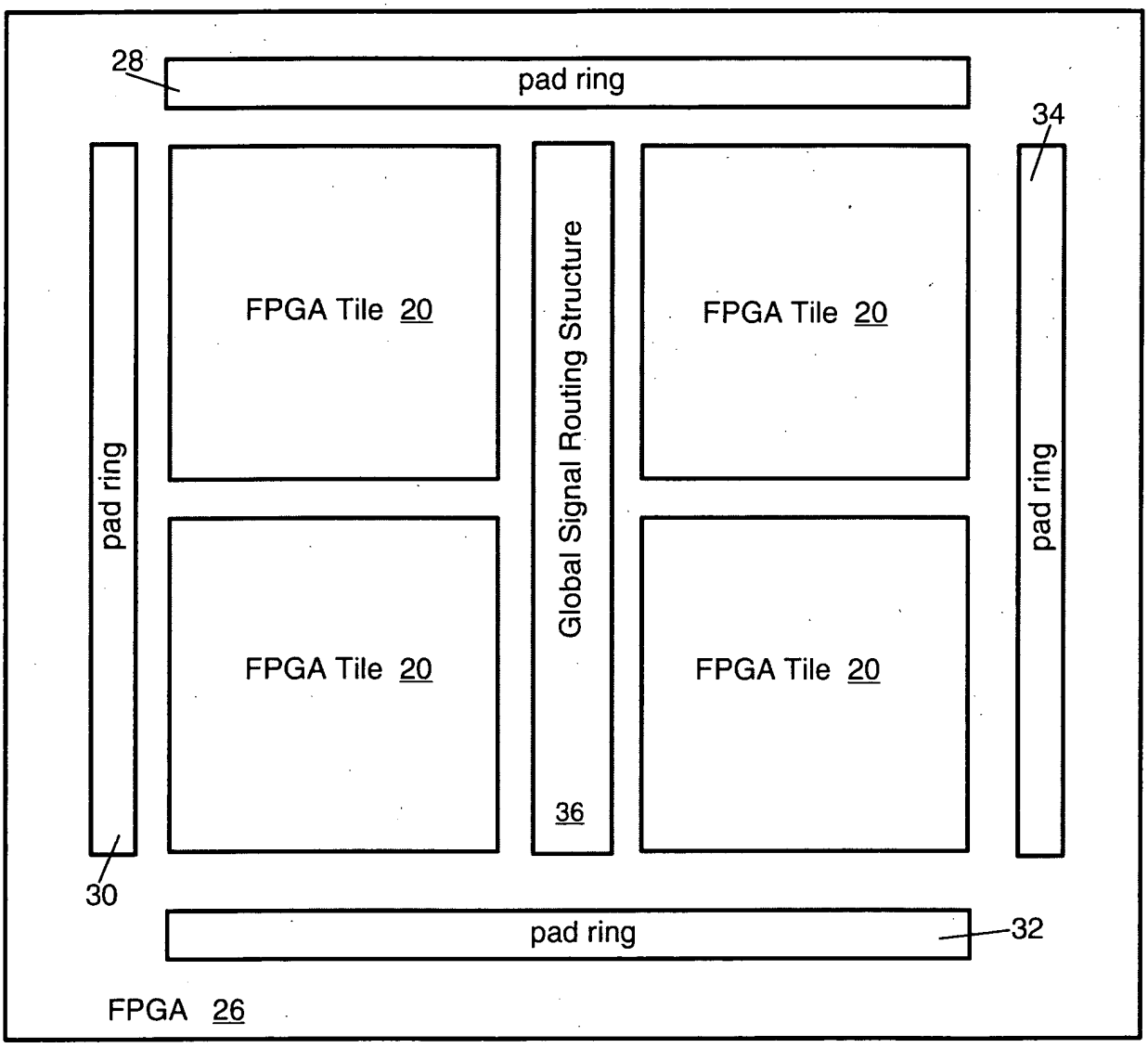
28
pad ring
34
FPGA Tile 20
Global Signal Routing Structure
FPGA Tile 20
pad ring
pad ring
FPGA Tile 20
FPGA Tile 20
36
30
pad ring
32
FPGA 26

FIG. 4

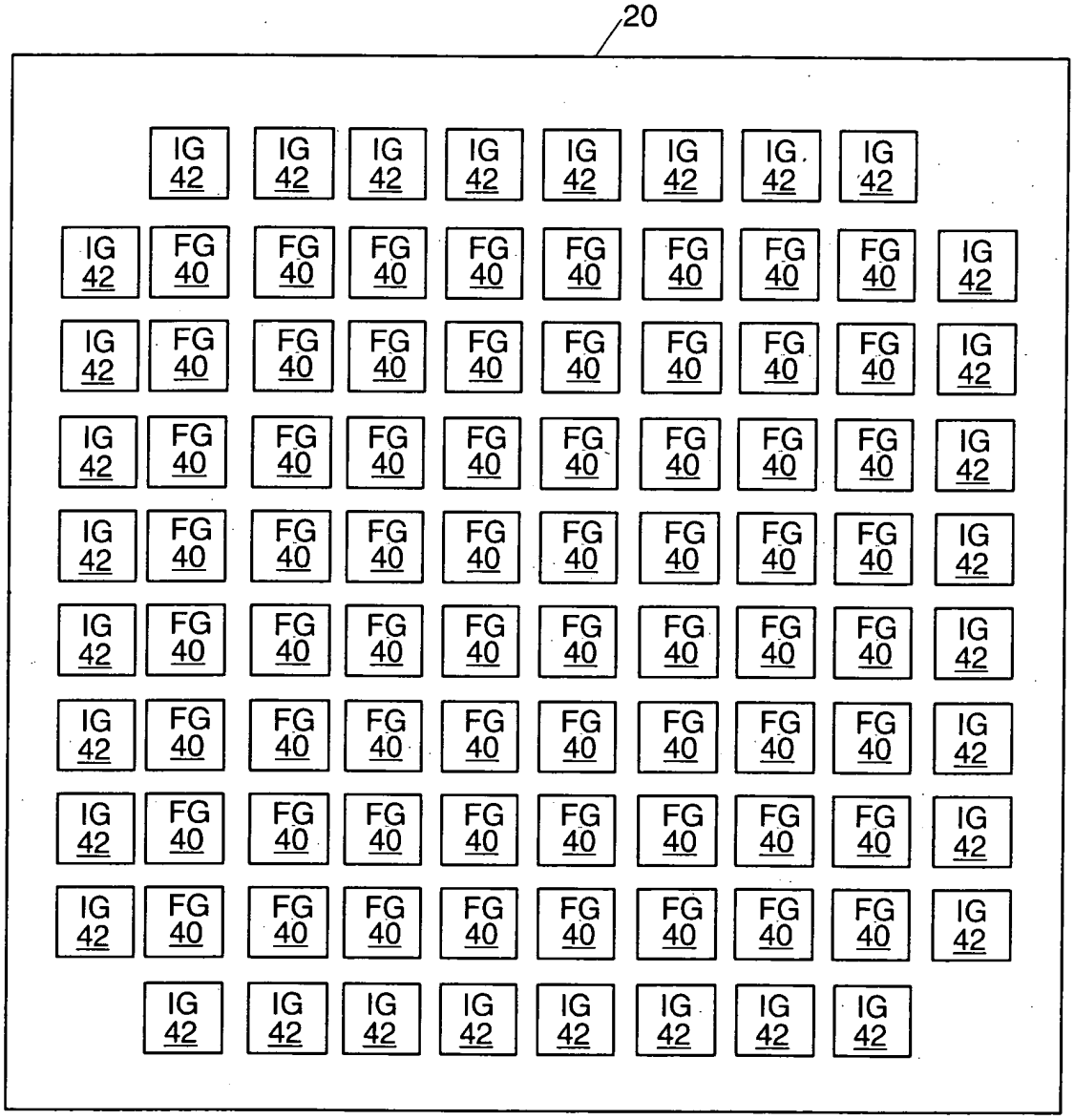

FIG. 5

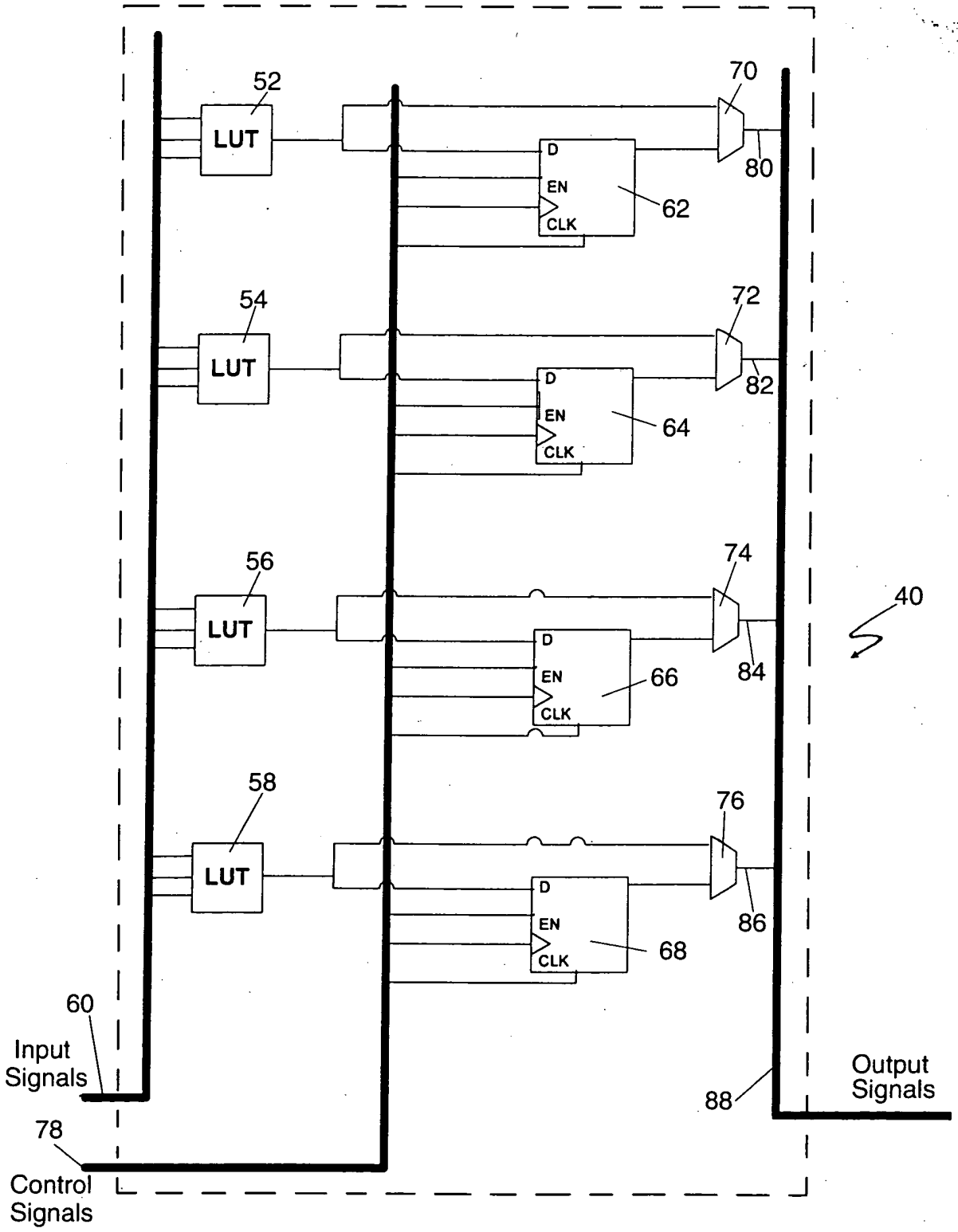
52
LUT
70
D
EN
CLK
62
80
54
LUT
72
D
EN
CLK
64
82
56
LUT
74
D
EN
CLK
66
84
40
58
LUT
76
D
EN
CLK
68
86
60
Input Signals
78
Control Signals
88
Output Signals

FIG. 6

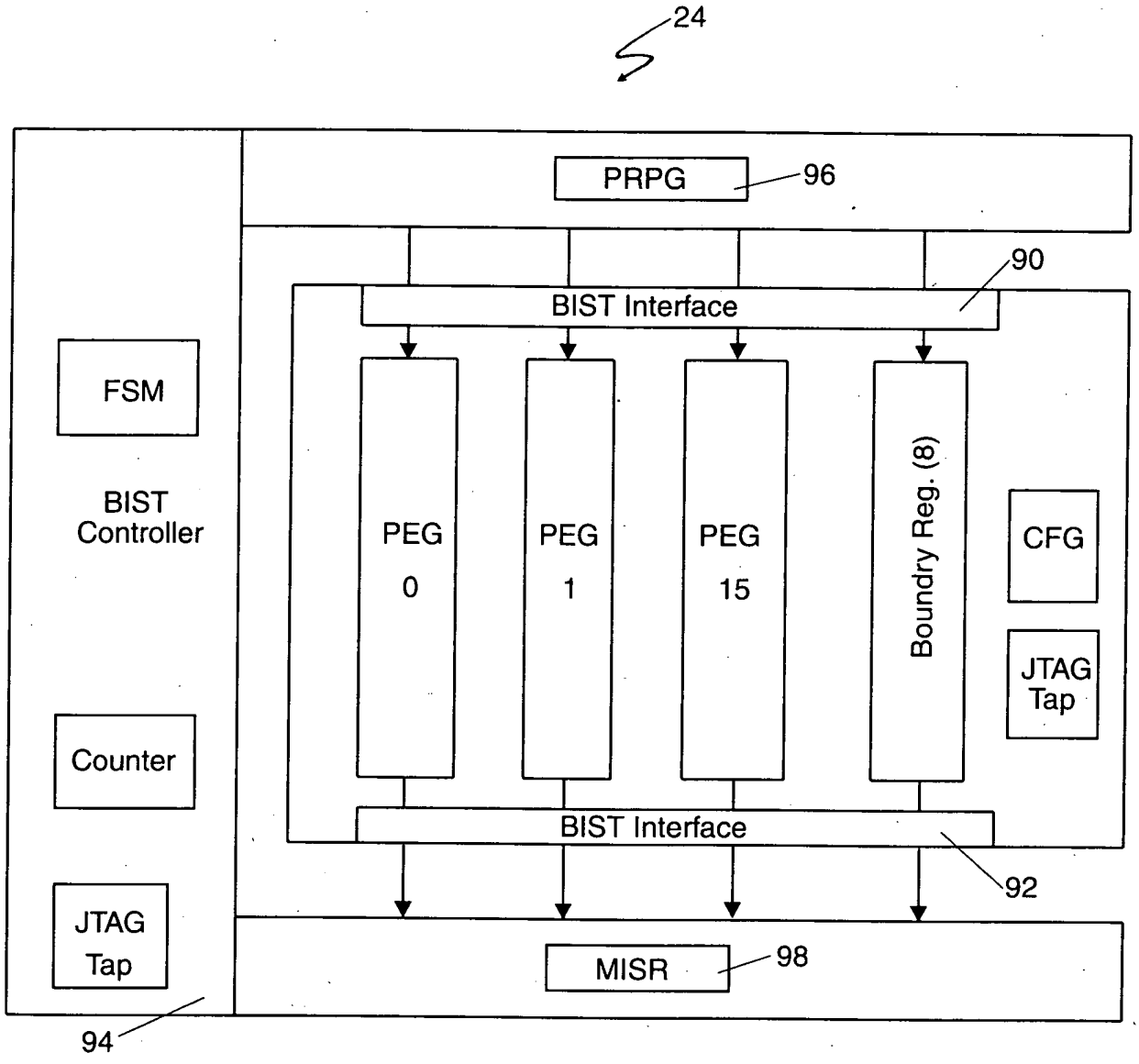
24
PRPG
96
90
BIST Interface
FSM
BIST
Controller
PEG
0
PEG
1
PEG
15
Boundry Reg. (8)
CFG
JTAG
Tap
Counter
BIST Interface
92
JTAG
Tap
MISR
98
94

FIG. 7

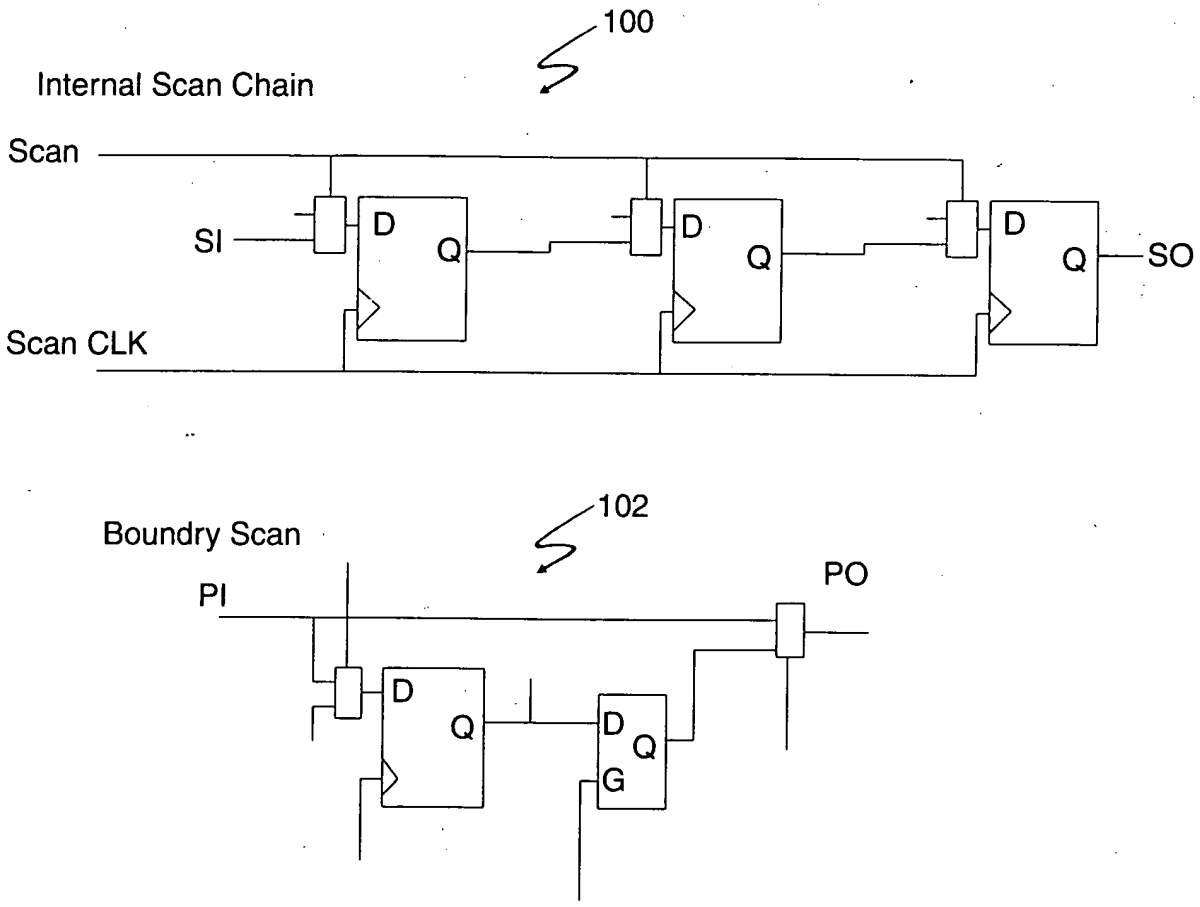
100
Internal Scan Chain
Scan
SI
D
Q
D
Q
D
Q
SO
Scan CLK
102
Boundry Scan
PI
PO
D
Q
D
Q
G

FIG. 8

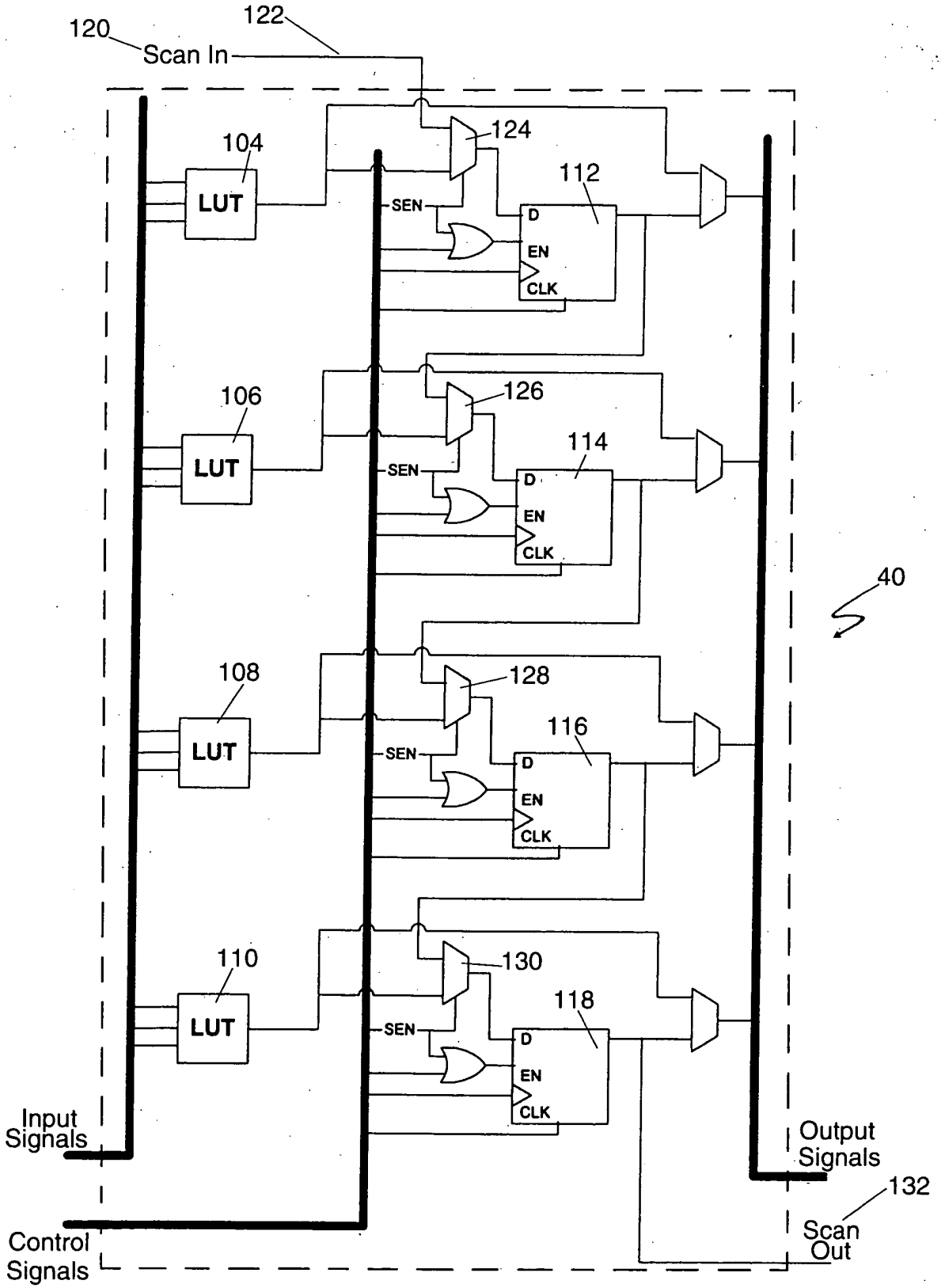
120
Scan In
122
104
LUT
124
112
SEN
D
EN
CLK
106
LUT
126
114
SEN
D
EN
CLK
40
108
LUT
128
116
SEN
D
EN
CLK
110
LUT
130
118
SEN
D
EN
CLK
Input Signals
Control Signals
Output Signals
132
Scan Out

FIG. 9

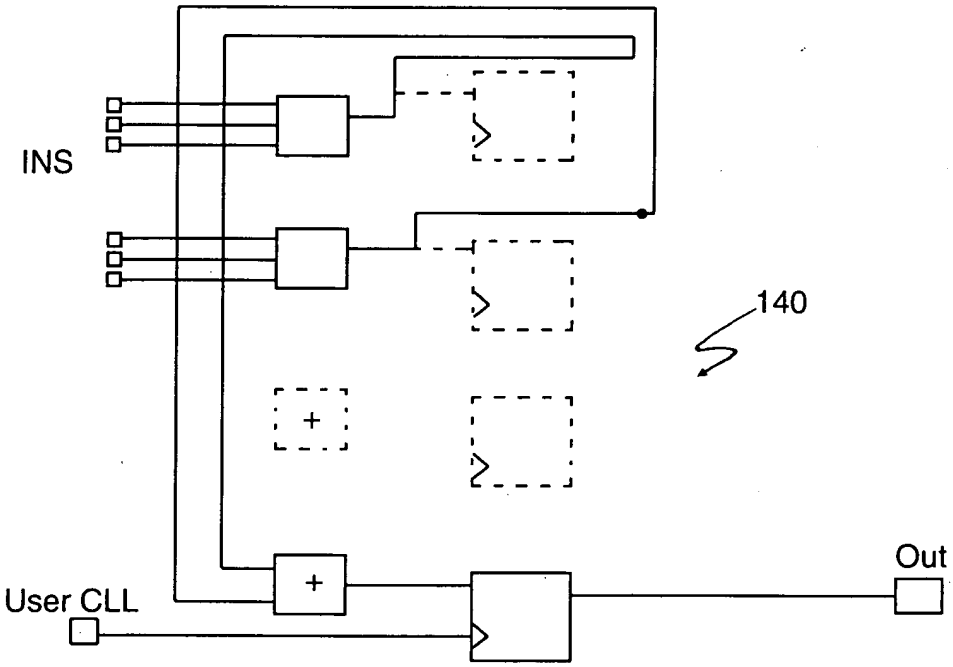

FIG. 10A

User Logic: Implemention of AND OR Circuit and Register

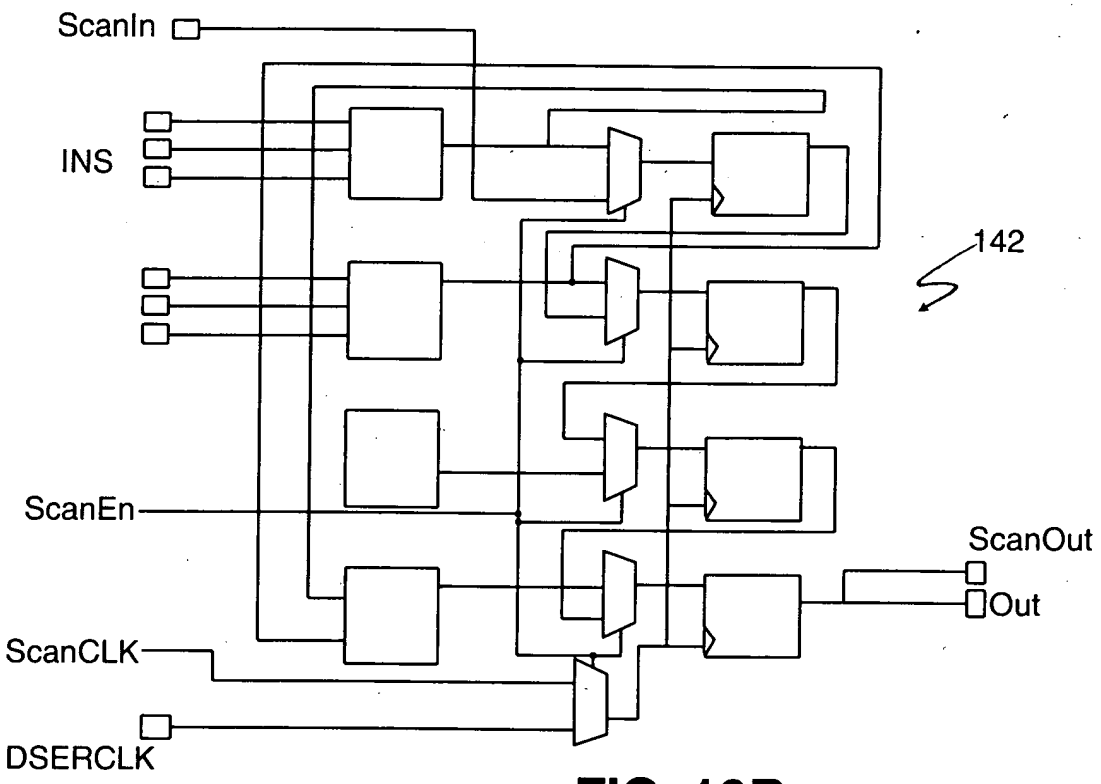

FIG. 10B

DSER Logic - with Scan Superimposed

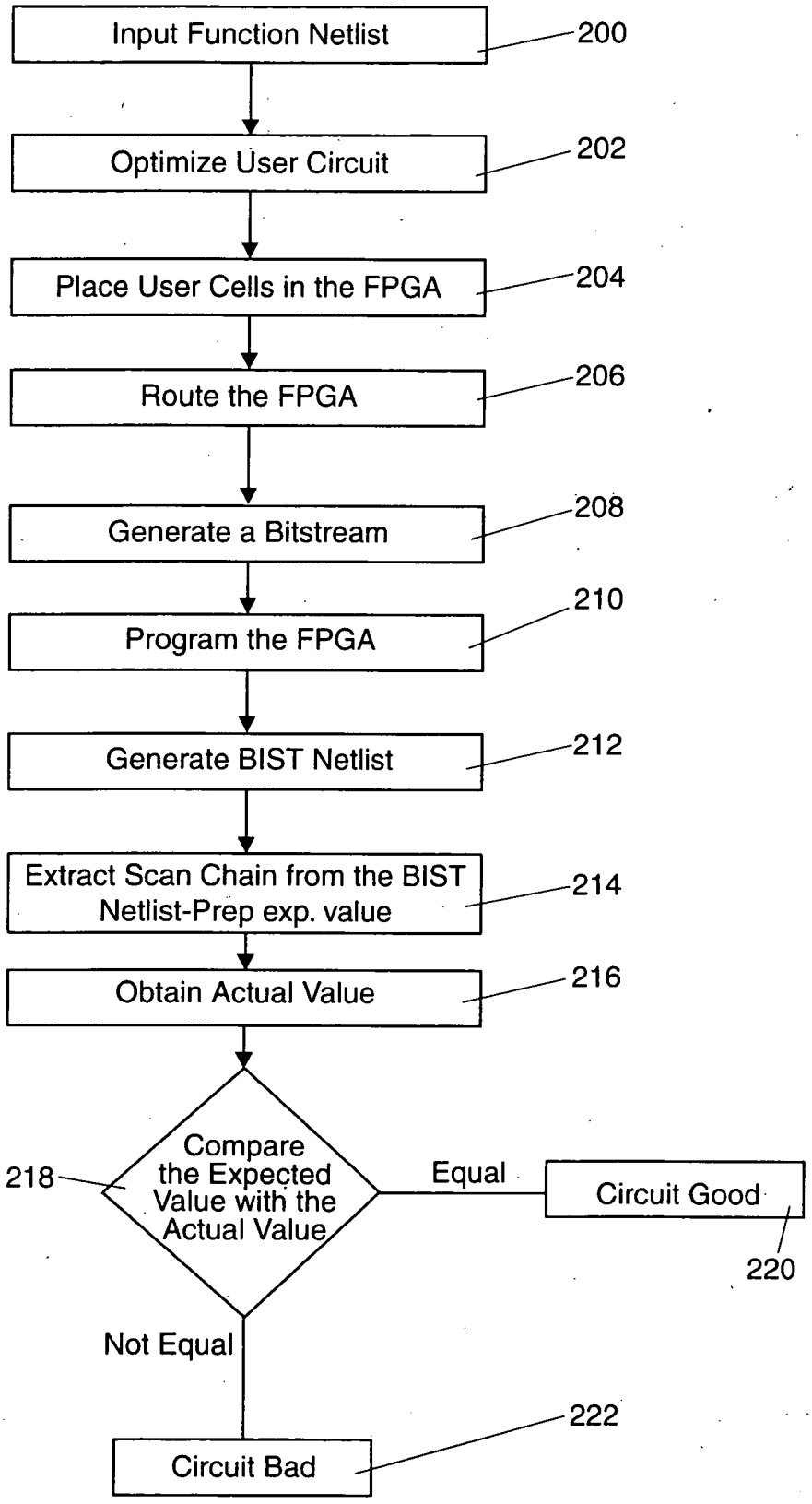
Input Function Netlist
200
Optimize User Circuit
202
Place User Cells in the FPGA
204
Route the FPGA
206
Generate a Bitstream
208
Program the FPGA
210
Generate BIST Netlist
212
Extract Scan Chain from the BIST Netlist-Prep exp. value
214
Obtain Actual Value
216
Compare the Expected Value with the Actual Value
218
Equal
Circuit Good
220
Not Equal
Circuit Bad
222

FIG. 11